Amendments to the Specification

Please replace the heading on page 1, line 5 with the following:

CROSS-REFERENCE TO RELATED APPLICATIONS

Please replace the heading on page 1, line 18 with the following:

BACKGROUND OF THE INVENTION

Please replace the heading on page 3, line 1 with the following:

SUMMARY OF THE INVENTION

Please replace the heading on page 4, line 1 with the following:

BRIEF DESCRIPTION OF THE DRAWINGS

Please replace the heading on page 5, line 1 with the following:

DETAILED DESCRIPTION OF THE INVENTION

Please replace the paragraph on page 8, lines 19-23 with the following paragraph:

The distributor unit 206 determines if a packet is ready for IPSec processing, and if so, distributes the security association information (SA) received from the packet classifier unit 204 and the packet data among a plurality of cryptography processing engines [[124]] 214, in this case four, on the chip 200, for security processing. This operation is described in more detail below.

Please replace the paragraph on page 10, line 33 - page 11, line11 with the following paragraph:

Fig. 3 is a block diagram of a cryptography accelerator chip architecture in accordance with one embodiment of the present invention. The chip 300 includes an input FIFO 302 into which IP packets are read. From the input FIFO 302, packet header information is sent to a packet classifier unit [[204]] 304 where a classification engine rapidly determines security association information required for processing the packet, such as encryption keys, data, etc. As described in further detail below, the classification engine performs lookups from databases stored in associated memory. The memory may be random access memory (RAM), for example, DRAM or SSRAM, in which case the chip includes a memory controller 308 to control the associated RAM. The associated memory may also be contact addressable memory (CAM), in which case the memory is connected directly with the cryptography engines 316 and packet classifier 304, and a memory controller is unnecessary. The associated memory may be on or off chip memory. The security association information determined by the packet classifier unit 304 is sent to a packet distributor unit 306 via the chip's internal bus 305.